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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant: Jianwei Liu § Art Unit: 2121
Serial No.: 09/966,022 §
Filed: September 28, 2001 § Examiner:
Title: Providing a Fast Adder for § Docket No. ITL.0648US
Processor Based Devices § (P12389)

Commissioner for Patents
Washington, DC 20231

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Technology Center 2100

Dear Sir:

This amendment corrects obvious typographical errors and does not introduce new material. Please amend the application as follows.

In the Specification:

Replace the paragraph beginning on line 2 of page 4 with the following:

One input pair (a_i, b_i) may or may not make a carry request. If two input pairs (a_i, b_i) and (a_j, b_j) are used, two carry requests may occur at the same time. Therefore, it is necessary to arbitrate these two carry requests. It is of note that i and j relate to two adjacent bits (at the first level) or blocks of bits (at subsequent levels) in the calculation, thus if we are arbitrating between carry requests relating to previously arbitrated blocks of 3 bits, then $i=j+3$.

Replace the paragraph beginning on line 15 of page 6 with the following:

The following equations satisfy Tables 3 and 4:

$$V_i = a_i b_i + (a_i + b_i) (a_j b_j + (a_j + b_j) a_k) \quad (3)$$

$$V_i = a_i b_i + (a_j + b_j) (a_j b_j + (a_j + b_j) b_k)$$

Date of Deposit: 09-27-02
I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated above and is addressed to the Commissioner for Patents, Washington, DC 20231.

Cindy Hayden